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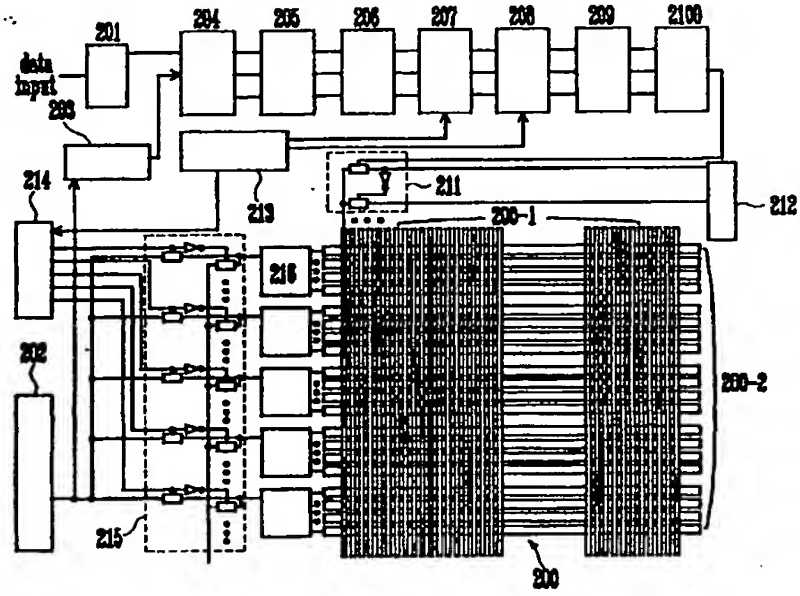

(57) Abstract

A super-twisted nematic liquid crystal display (STN-LCD) driving circuit adopting a multiple line selection method using pulse width modulation adopted to a driving circuit for a voltage driving flat panel display device, simplifies an LCD panel driving circuit, by applying a voltage whose pulse width, not magnitude, is modulated, to column lines of an STN-LCD panel, using two voltage potentials.

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SUPER-TWISTED NEMATIC LIQUID CRYSTAL DISPLAY DRIVING CIRCUIT ADOPTING MULTIPLE LINE SELECTION METHOD USING PULSE WIDTH MODULATION

TECHNICAL FIELD

The present invention relates to a super-twisted nematic liquid crystal display (STN-LCD) driving circuit adopting a multiple line selection method using pulse width modulation using a driving circuit for a voltage driving flat panel display device, and more particularly, to an STN-LCD driving circuit adopting a multiple line selection method using pulse width modulation, which simplifies an LCD panel driving circuit, by applying a voltage whose pulse width, not magnitude, is modulated, to column lines of an STN-LCD panel, using two voltage potentials.

BACKGROUND ART

In general, a voltage driving display panel is classified into a thin film transistor liquid crystal display (TFT-LCD) panel using an active matrix addressing method, and an STN-LCD panel using a passive matrix addressing method, both of which display a picture image by intermitting a light source using liquid crystals.

The TFT-LCD panel controls each pixel by using the active matrix addressing method using a transistor serving as a switch and a storage capacitor for each pixel for the purpose of displaying a picture image on a liquid crystal display panel, which is advantageous in implementing clear picture quality. However, the transistor and capacitor should be implemented on a glass plate of the LCD panel, which costs much.

The structure of the STN-LCD panel using the passive matrix addressing method is shown in FIG. 1, in which transparent electrodes 20 and 21 orthogonally crossing with each other are placed between two glass substrate 10 and 11 and orientation films 30 and 31 are coated on the transparent electrodes 20 and 21 to orientate liquid crystals 40.

The orientation films 30 and 31 fix the liquid crystals 40 unidirectionally between the glass substrates 10 and 11, because it is difficult to orientate the liquid crystals 40 by using only the glass substrates 10 and 11. The liquid crystals 40 are in a nematic state, the unit molecular thereof is long and flat, and are aligned horizontally with respect to a major axis.

The ends of the long molecules form their combination by Van Der Waals' force.

The light passing through the afore-constructed STN-LCD panel is twisted locally in its optical axis by optical anisometric property, that is, different refractive indexes, as shown in FIGs. 2A and 2B. Then, the light passes through an outer surface of the glass substrate 10 and 11 by an orthogonally fixed polarizing plate 50.

The light passing through the STN-LCD panel exhibits intrinsic colors by speed difference depending on the light traveling direction in the course of passing the liquid crystals 40. Since such intrinsic colors impede expression of colors on the liquid crystals, the intrinsic colors should be deleted by reducing the speed difference. A delay film 60 shown in FIG. 1 is used for correcting the speed difference.

In such a state, if a voltage is applied to the transparent electrodes 20 and 21 of the STN-LCD panel, the liquid crystals are aligned in a direction of electrical fields, as similarly as shown in FIG. 2B, to then shield the light. The twisting degree of the liquid crystals in the STN-LCD panel reaches 240~270°, which is larger than that shown in FIG. 2 showing a twisted nematic liquid crystal display (TN-LCD) panel.

The STN-LCD panel having the aforementioned characteristics can be implemented at low cost, compared to the TFT-LCD panel, since no element is required other than a capacitor component of the liquid crystals themselves. However, since a pixel is positioned at a point where two matrix-typed electrode lines intersect with each other and the liquid crystals operate by the difference in voltages

applied to the electrode lines, there is no element for reducing the effect on ambient pixels, which causes picture quality to be reduced.

To solve the above-described shortcoming, there has been proposed a conventional driving method for displaying a high-quality moving picture in the STN-LCD panel, which will now be described with reference to FIG. 3.

The LCD driver shown in FIG. 3 includes a buffer 80 for storing input data as picture information in the unit of frames, an ROM for a row function 81 for generating a Walsh function so as to operate row lines of an STN-LCD panel 90, a register 82 for storing the Walsh function output from the ROM for a row function 81, an operating portion 83 for receiving tow signals output from the buffer 80 and register 82 and performing an exclusive OR (XOR) operation, a sum logic portion 84 for accumulating values output from the operating portion 83 and outputting a voltage to a voltage source portion 85 so that the voltage is applied to column lines of the STN-LCD panel 90, the voltage source portion 85 having a plurality of voltage potential levels applied to the column lines set therein, for supplying a voltage corresponding to a value input from the sum logic portion 84, and a level shifter 86 for level-shifting the row function output from the register 82 so as to apply the same to the row lines.

The STN-LCD panel 90 includes a plurality of column lines 91 and a plurality of row lines 92 for displaying picture information, and a plurality of pixels 93 formed at the respective intersection points of the column lines 91 and row lines 92.

The data stored in the buffer 80 expresses information to be displayed by the pixels 93, which is represented by -1 when the pixels 93 operate (ON) and is represented by +1 when the pixels 93 do not operate (OFF).

The operational procedure of the STN-LCD panel driver having the aforementioned configuration will now be described. The picture information to be displayed on the LCD is stored in the buffer 80 and at the same time a Walsh

function, i.e., an orthogonal function, is outputted from the ROM for a row function 81 to be stored in the register 82 for execution of the XOR operation, which is inputted to the level shifter 86 so as to select all row lines of the LCD panel.

In such a state, if the data and function value stored in the buffer 80 and register 82 are inputted to the operating portion 83, respectively, the operating portion 83 performs an XOR operation with respect to the two input values to then output the respective potential values of a column line corresponding to each row line to the sum logic portion 84. The sum logic portion 84 accumulatively operates these values to then output the same as values corresponding to the voltage values applied to the column lines.

If the result values of the sum logic portion 84 are outputted, the voltage source portion 85 applies the voltage corresponding to the result values to the respective column lines, and at the same time, the Walsh function value input to the level shifter 86 is level-shifted to apply a voltage to the row lines.

In this manner, if a voltage is applied to each row line and column line, the intended picture information is displayed on the LCD panel.

Now, the Walsh function used in the aforementioned driving circuit will be described for reference. The Walsh function is shown in FIG. 5, which is an orthogonal function, whose logic values iterate +1 and -1. The respective waveforms shown in FIG. 5 (1~n) are applied to the respective row lines 92 by the ROM for a row function 81. Also, if the respective waveforms (1~n) are multiplied with one another to be integrated in one period, a result value of logic '0' is output.

The function having such characteristics is used for reducing the effect of the interference between the respective lines by the voltage applied to the row lines while driving the row lines.

The voltage applied to the respective column lines 91,

as described above, allows the data signal and Walsh function to be XOR-operated by the operating portion 83. Then, a predetermined voltage potential applied externally by the operation result of the sum logic portion 84 is used. The operation result is expressed by $D_j(\Delta t_k)$ in FIG. 3. The value of $D_j(\Delta t_k)$ is obtained by adding the logic value of the Walsh function applied to the row lines 92 with the number of cases where the logic values of data correspond to each other, which follows a Gaussian distribution statistically. In the case of driving in the conventional manner, when the number of the row lines 92 is 240, the convergence range of $D_j(\Delta t_k)$ falls within 45 with 120 centered.

As described above, according to the driving method proposed to implement a high-quality moving picture in the slowly responsive STN-LCD panel, the row lines are driven at once, which is because it is difficult to implement a moving picture in the slowly responsive STN-LCD panel by using the conventional method. The number of voltage potentials applied to the column lines 91 in driving the LCD panel in the aforementioned manner is the same as that of convergent ranges of $D_j(\Delta t_k)$, which is called an active addressing method.

However, according to the active addressing method, it is very difficult to implement the number of voltage potentials actually necessary in a hardware manner.

As a similar method to the active addressing method, a method of determining the magnitude of voltage potentials in the same manner as the active addressing method and reducing the number of necessary voltage potentials by defining row lines driven at once as a row line group of a predetermined number, not all lines, which is particularly called a multiple line selection (MLS) method, as shown in FIG. 4 has been proposed. FIG. 4 is an enlarged view of a panel portion and a row line portion of the STN-LCD panel shown in FIG. 3. The other parts are the same as those shown in FIG. 3 and thus, an explanation thereof will be omitted.

The LCD driver shown in FIG. 4 includes an ROM for a row function 100 for providing a Walsh function, level

shifters 120 and 130 each connected to a plurality of row line groups, shift register 110 for switching to operate the level shifter connected to a selected row line group from the respective level shifters 120 and 130, and an STN-LCD panel 140 comprised of a plurality of column lines 141, a plurality of row line groups 142 having a predetermined number of groups, and a plurality of pixels 143.

The operation of the LCD panel driver having the aforementioned configuration is almost the same as that explained with reference to FIG. 3, and is only different in that all row lines are not selected at once but divided row line groups are selectively driven.

In other words, when a row line group is selected, the other row line groups are not selected. Such an MLS method reduces the number of voltage potentials to be implemented in a hardware manner, compared with the active addressing method. However, this method should also implement multiple voltage potentials in a hardware manner.

DISCLOSURE OF THE INVENTION

Therefore, it is an object of the present invention to provide a new LCD driving method for implementing picture quality similar to that of a TFT-LCD panel by using a cheap STN-LCD panel.

In other words, according to the present invention, in applying a voltage to an LCD device, a lot of predetermined voltage potentials are not applied but two voltage potentials are determined previously to then adjust the widths of pulses having the respective voltage potentials according to operated logics, and to adjust a valid voltage value for duration of one frame, thereby compensating for shortcomings of the active addressing method and MLS method.

To accomplish the above object of the present invention, in a liquid crystal display device having a plurality of column lines, a plurality of row lines, and pixels each formed at a point where the column lines and row lines intersect with each other, there is provided an STN-LCD panel driving circuit adopting a multiple line selection

(MLS) voltage applying method using pulse width modulation, comprising: a decoder for receiving a value output from an adder for accumulating to-be-displayed data and XOR-operated values of an orthogonal function and decoding the same into a value being in a state where the value is capable of being pulse-width-modulated; a first buffer for sequentially storing a value modulated from the decoder; a second buffer for re-storing values for a to-be-operated column line which are stored in the first buffer at once; a MUX portion for selectively outputting values stored in the second buffer bit by bit; a flipflop portion for turning on a gate corresponding to a column line selected by the MUX portion so as to supply a ready voltage potential to the selected column line; a voltage source portion having two voltage potential values applied to the column line set therein, and connected to the gate turned on by the operation of the flip flop portion for applying a voltage to the column line; and a clock circuit for supplying a reference clock to the respective buffers and to a selection switch, wherein a voltage is supplied to column lines by using two voltage potentials.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a sectional view showing a conventional STN-LCD panel;

FIG. 2 explains a twist pattern of light passing through a polarizing plate according to liquid crystals in the conventional STN-LCD panel;

FIG. 3 is a block diagram of a LCD driving circuit using a conventional active addressing method;

FIG. 4 is a block diagram showing a row-line selecting portion in the LCD driving circuit using the conventional multiple line selection method;

FIG. 5 is a waveform diagram of an orthogonal function applied to row lines;

FIG. 6 explains a voltage applied to column lines by modulating a pulse width during a temporal interval of τ shown in FIG. 5;

FIG. 7 is a block diagram of a LCD driving circuit implemented by the present invention; and

FIG. 8 is a timing diagram showing an output timing of a clock circuit according to the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

In the present invention, in order to determine the number of row lines driven at once, the above-described MLS method (see FIG. 4) is adopted, and a voltage applied to a selected column line is pulse-width-modulated, as shown in FIG. 6.

Also, a Walsh function which is an orthogonal function applied to a selected row line group is divided in a predetermined number of time intervals τ, as shown in FIG. 5. Voltages a and c applied to the selected row line group repeatedly take logic values +1 and -1 for duration of τ, and the magnitude thereof is maintained as F and -F (see FIG. 6).

A voltage having a magnitude of '0' is applied to non-selected row line groups while the Walsh function is being applied thereto.

Also, the voltage applied to the column line for the time intervals τ takes a value of eF for a predetermined time period by the operation of data and Walsh function applied to the selected row line group, and takes a value of -eF for the other time periods. A reference character L represents a value determined so that values up to 2σ are contained among the operation results of a row line signal having Gaussian distribution and a picture signal, and a reference character b is a value for determining a modulation point of a voltage applied to the column line according to the result of a sum logic operation.

The reason why the magnitude of a signal applied to the column line is set to eF and e is set to a value between 0 and 1 will now be described.

According to the MLS method, in driving a predetermined number of selected row line groups, the remaining row line groups are not driven.

In other words, after data signals for the row line groups are operated by an operating portion, data signals for the remaining non-selected row line groups are not taken into consideration while being applied to the column line.

However, since the STN-LCD panel adopts a passive addressing method, a voltage value irrespective to the data signal of a pixel connected to the non-selected row line group is applied to the pixel,

Also, in driving the STN-LCD panel, the liquid crystals 40 are driven by a valid voltage level applied thereto during the period of one frame. In the case of adopting the MLS method, while the selected row line groups are driven, the voltage applied to the pixel influences the magnitude of the valid voltage during the period of one frame.

Therefore, in order to control the valid voltage applied to the pixel for one frame exactly when using the MLS method, it is important that the magnitude of the voltage applied while no row line group is selected is made as small as possible so that the influence upon the magnitude of the valid voltage for one frame is reduced.

Therefore, according to the present invention, a voltage whose magnitude is zero is applied to a non-selected row line, so that the valid voltage applied to a pixel for non-selection time becomes eF which is applied to the column line and the influence upon the magnitude of the valid voltage for one frame is reduced by defining the value of e as a value coming between 0 and 1.

As described above, in the MLS STN-LCD driving method using pulse width modulation, the valid voltage applied to the pixel for one frame is obtained by the following formula:

$$\langle V\rangle^2 = \frac{F^2\left(1+e^2-\frac{2e}{L}d_i\right)+\frac{N-S}{S}e^2F^2}{N/S} - \frac{F^2\left(1+\frac{N}{S}e^2-\frac{2e}{L}d_i\right)}{N/S}$$

where F represents the magnitude of a row line signal, N represents the total number of the row lines, S represents the number of the row line selected at once, eF represents the magnitude of a column line signal, L represents the number of time units in which a voltage applied to a column line for time intervals τ is modulated, and d_i represents a data signal for a pixel positioned at an ith row line in a selected row line group.

The values of the above formula are determined to have the maximum value in the ratio of voltages applied when a pixel operates and when the pixel does not operate.

Here, an on/off ratio of the liquid crystals is about 1.06 and the maximum value in the case when S is 9 and L is 6 is about 1.03.

The LCD driving circuit implemented by adopting the aforementioned method, as shown in FIG. 7, includes a buffer 201 for storing picture information as input data in the unit of frames, an ROM for a Walsh function 201 for generating a Walsh function so as to operate a row line on an STN-LCD panel 200, a register 203 for storing a Walsh function value output from the ROM for a Walsh function 201, an operating portion 204 for receiving two signals output from the buffer 201 and ROM for a Walsh function 202 and performing an XOR operation with respect to the two signals, an adder 205 for accumulating values output from the operating portion 204 so as to apply a voltage to a column line in liquid crystals, a decoder 206 for pulse-width-modulating a value output from the adder 205 and decoding the same into a value being in the state where the value is capable of being pulse-width-modulated, to then be applied to the liquid crystals, a first buffer 207 for sequentially storing a value modulated from the decoder 206, a second buffer 208 for re-storing values for a to-be-operated column line which are stored in the first buffer 207 at once, a MUX portion 209 for selectively outputting values stored in the second buffer 208 bit by bit, a T-flipflop portion 210 for turning on a gate corresponding to a column line selected by the MUX portion 209 in a second gate portion 211 so as to

supply a ready voltage potential to the selected column line, a voltage source portion 212 having two voltage potential values applied to the column line set therein, and connected to the gate turned on by the operation of the T-flipflop portion 210 for applying a voltage to the column line, a clock circuit 213 for supplying a reference clock to the respective buffers 207 and 208 and to a selection switch 214, the selection switch 214 for selecting a row line groups among a plurality of row line groups 200-2 according to the state of a clock output from the clock circuit 213, a plurality of first gate portions 215 for allowing a voltage to be applied to the row line group by turning on the gate according to the signal output from the selection switch 214, level shifters 216 each for level-shifting so as to apply a Walsh function value applied through the gate turned on by the selection switch among the plurality of first gate portions 215, and an LCD device 200 comprised of a plurality of column lines 200-1, a plurality of row line groups 200-2 and a plurality of pixels (not shown) formed at the respective intersection points of the column lines 200-1 and row line groups 200-2.

The operation of the driving circuit having the aforementioned configuration will now be described. In other words, data to be displayed is stored in the buffer 201, and the Walsh function is output from the ROM for the Walsh function 202.

The respective signals are input to the operating portion 204 to then be XOR operated and added in the adder 205, which is then input to the decoder 206. The value input to the decoder 206 is output in the form of $D_j(\Delta t_k)$, as described in the conventional art.

The decoder 206 receives the value, aligns the received value in the unit of bits and outputs the same. For example, when the output value is 5 and is output in the unit of 10 bits, the value is output in the data form of 0000010000.

If the output values are sequentially stored in the first buffer 207 in tune with the clock A (FIG. 8(d)) output

from the clock circuit 213 and the operation result values for column lines to-be-operated are all stored and the values are all output to the second buffer 208 in accordance with the clock B (FIG. 8(b)) output from the clock circuit 213.

FIG. 8 is a timing diagram showing waveforms when data of 120 column lines are processed at once, in which the clock A (FIG. 8A) represents a basic clock for the 120 column lines, the clock C (FIG. 8(c)) is for generating a Walsh function for performing an operation with respect to a data signal and a row line signal, and the clock D (FIG. 8(d)) is a waveform for generating the Walsh function applied to the row line, in which the Walsh function for operation leads that applied to the row line by one clock.

As described above, the result values are stored by using two buffers 207 and 208 for continuously performing the Walsh functional operation and applying a voltage to the LCD panel, thereby preventing the speed from being lowered by the increased operation quantity.

Subsequently, the result values stored in the second buffer 208 are outputted bit by bit by the MUX portion 209 and allows the corresponding gate among the plurality of second gate portions 215 connected to the voltage source portion 212 via the T-flipflop portion 210 to be turned on. A voltage is set externally through the voltage source portion 212 connected to the turned on gate to the column line.

Also, the Walsh functions generated from the ROM 202 for the Walsh function are sequentially applied to the row line group selected by the selection switch 214 according to the clock applied from the clock circuit 213 so that the pixel intersecting with the column line is displayed.

As described above, according to the present invention, since a voltage is applied to a column line by modulating the width of its pulse, not the magnitude thereof, for implementing a high-quality moving picture in an STN-LCD panel, the LCD device can be driven by using two voltage potentials, which simplifies hardware configuration.

INDUSTRIAL APPLICABILITY

The present invention can be applied to a driving circuit for a voltage driving flat panel display device.

WHAT IS CLAIMED IS:

1. In a liquid crystal display device having a plurality of column lines, a plurality of row lines, and pixels each formed at a point where the column lines and row lines intersect with each other, a super-twisted nematic liquid crystal display (STN-LCD) panel driving circuit adopting a multiple line selection (MLS) voltage applying method using pulse width modulation, comprising:

a decoder for receiving a value output from an adder for accumulating to-be-displayed data and XOR-operated values of an orthogonal function and decoding the same into a value being in a state where said value is capable of being pulse-width-modulated;

a first buffer for sequentially storing a value modulated from said decoder;

a second buffer for re-storing values for a to-be-operated column line which are stored in said first buffer at once;

a multiplexer (MUX) portion for selectively outputting values stored in said second buffer bit by bit;

a flipflop portion for turning on a gate corresponding to a column line selected by said MUX portion so as to supply a ready voltage potential to said selected column line;

a voltage source portion having two voltage potential values applied to said column line set therein, and connected to the gate turned on by the operation of said flipflop portion for applying a voltage to said column line; and

a clock circuit for supplying a reference clock to said respective buffers and to a selection switch, wherein a voltage is supplied to column lines by using two voltage potentials.

2. A super-twisted nematic liquid crystal display (STN-LCD) panel driving circuit as claimed in claim 1, wherein said clock circuit sequentially controls enabling operations of said first and second buffers to prevent the speed of

said LCD driving circuit from being lowered by increased operation quantity.

3. A super-twisted nematic liquid crystal display (STN-LCD) panel driving circuit as claimed in claim 1, wherein said clock circuit has two voltage potential values set therein, and a valid voltage for determining the magnitude of the voltage applied to said column line by modulating the pulse width of said voltage potentials, the magnitude of the voltage applied to said row line and the number of time intervals is obtained by the following formula:

$$\langle V\rangle^2 = \frac{F^2\left(1+e^2-\frac{2e}{L}d_i\right)+\frac{N-S}{S}e^2F^2}{N/S} - \frac{F^2\left(1+\frac{N}{S}e^2-\frac{2e}{L}d_i\right)}{N/S}$$

where F represents the magnitude of a row line signal, N represents the total number of said row lines, S represents the number of the row line selected at once, eF represents the magnitude of a column line signal, L represents the number of time units in which a voltage applied to the column line for time intervals τ is modulated, and d_i represents a data signal for a pixel positioned at an ith row line in a selected row line group.

4. A super-twisted nematic liquid crystal display (STN-LCD) panel driving circuit as claimed in claim 3, wherein the factor influencing the magnitude of a valid voltage for one frame is reduced by defining the value of e as a value coming between 0 and 1 in order to reduce the magnitude of a voltage applied to a pixel while no row line group is selected.

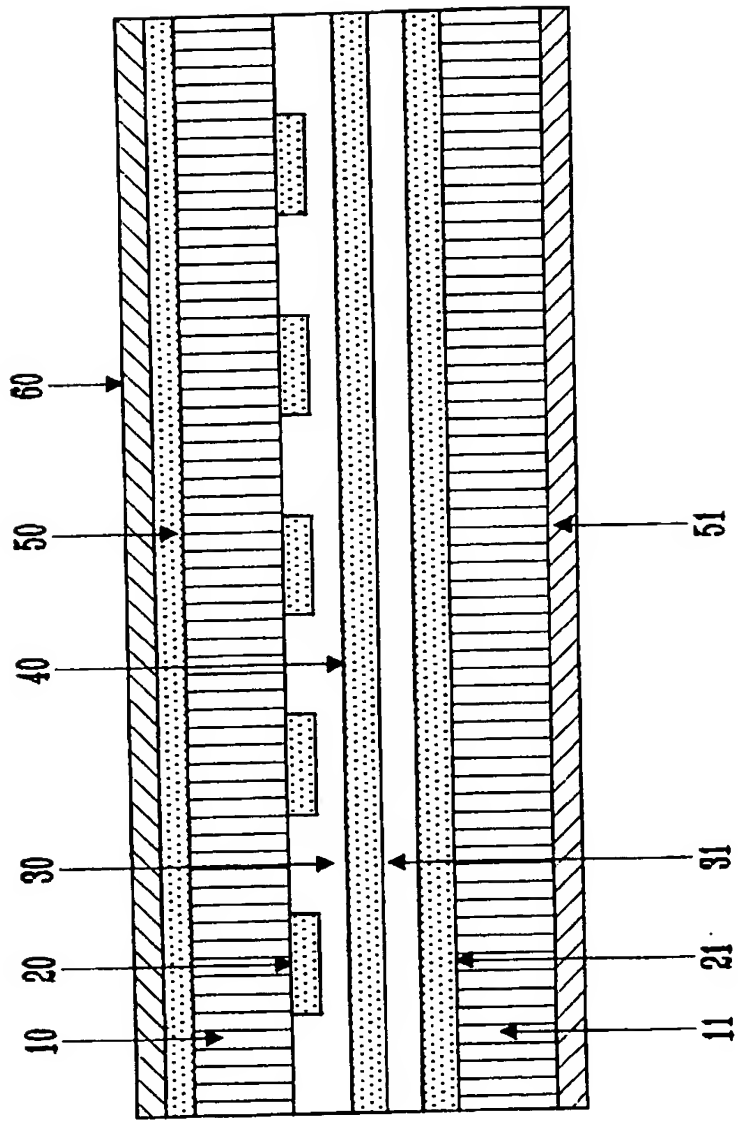

Fig. 1

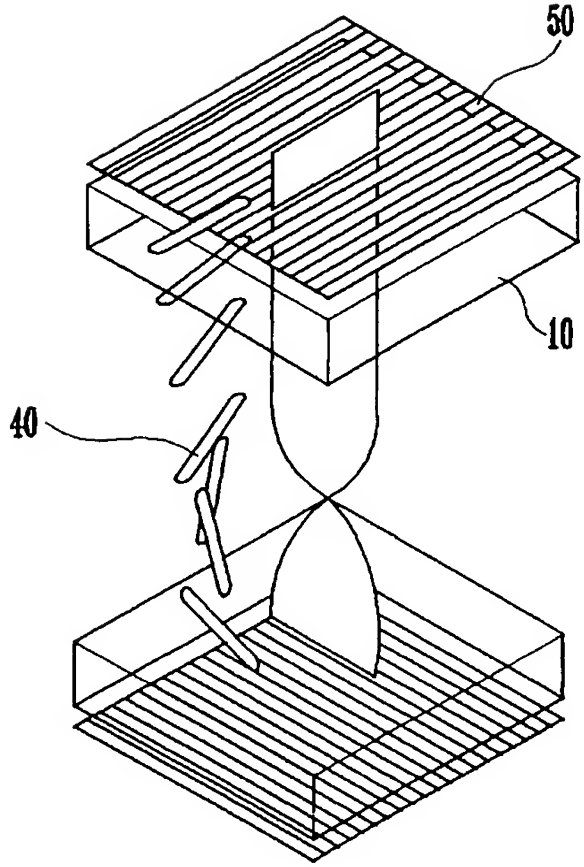

Fig . 2A

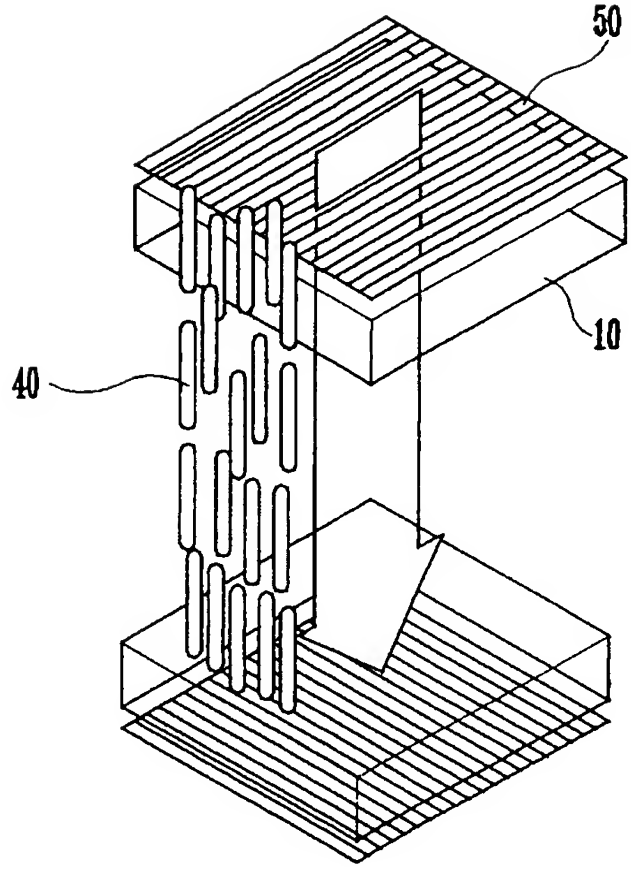

Fig . 2B

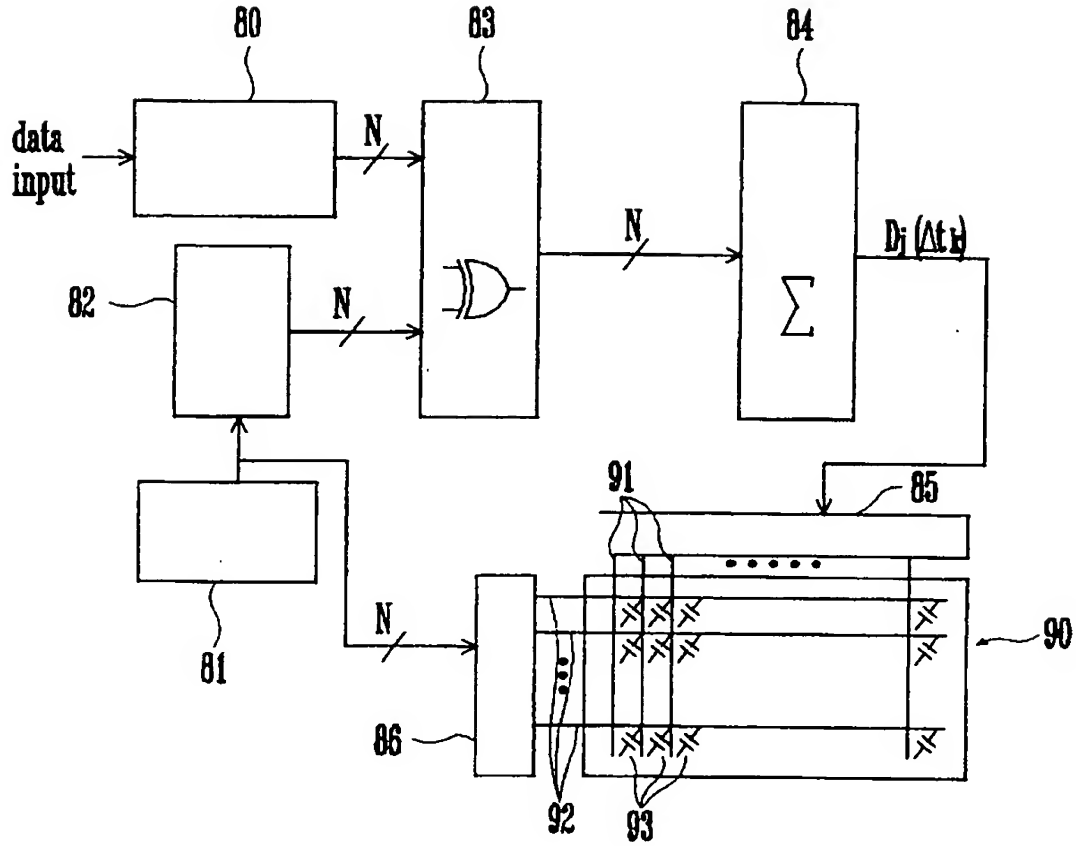

Fig . 3

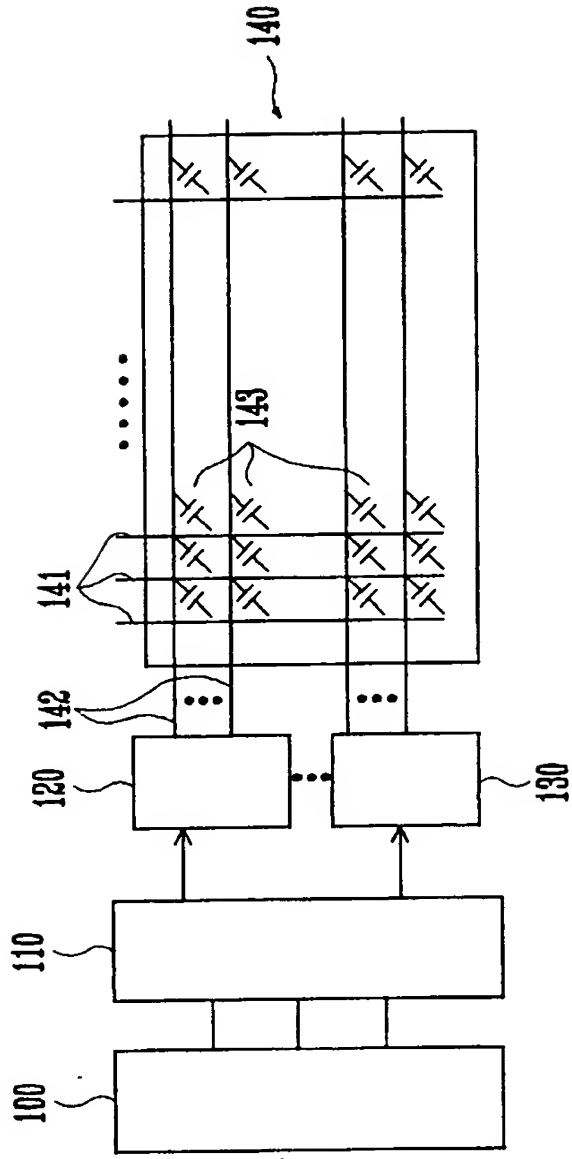

Fig. 4

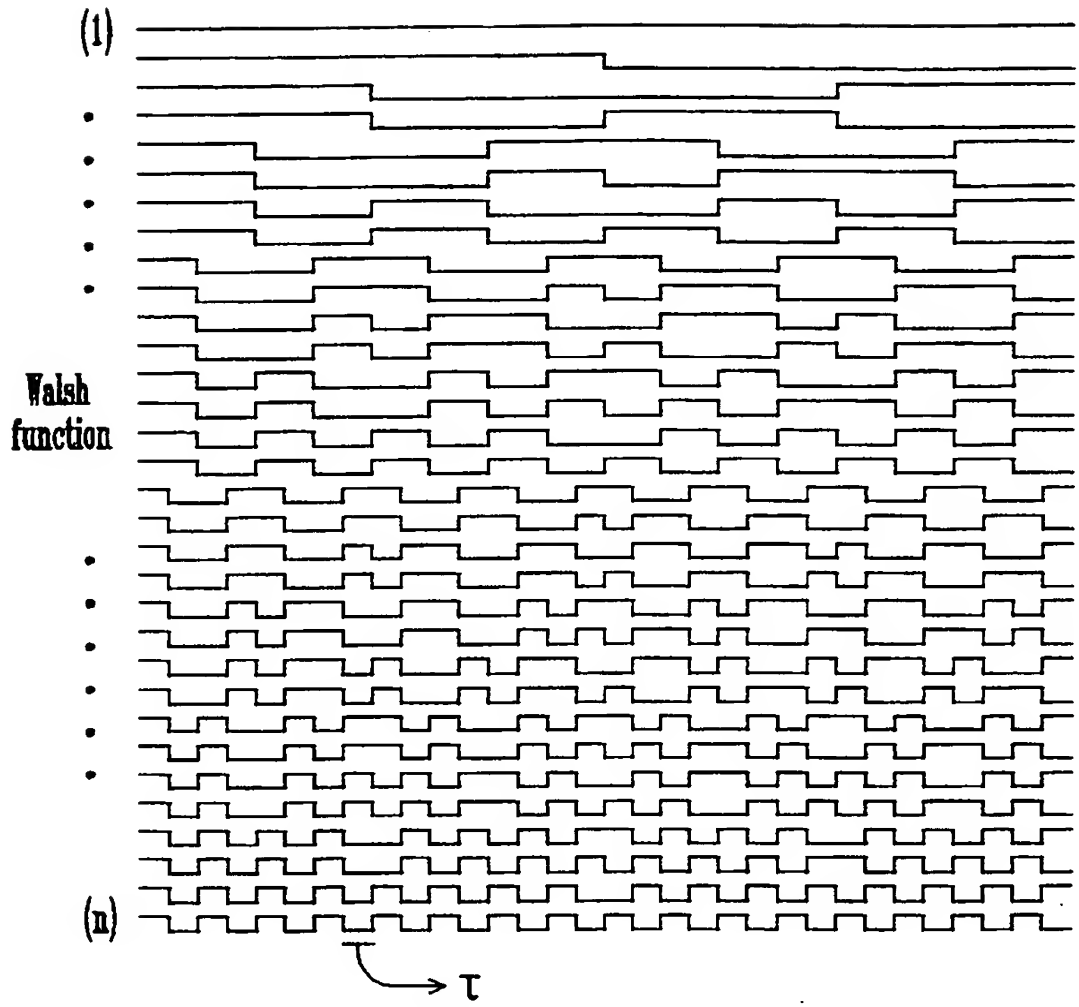

Fig . 5

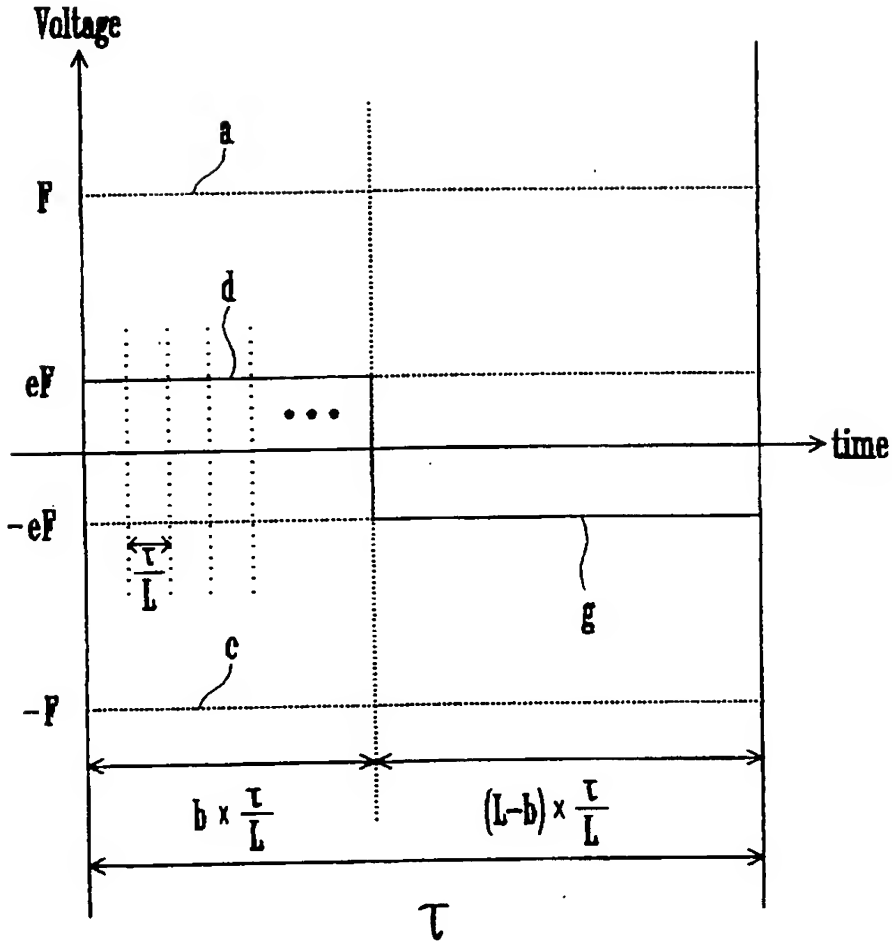

Fig . 6

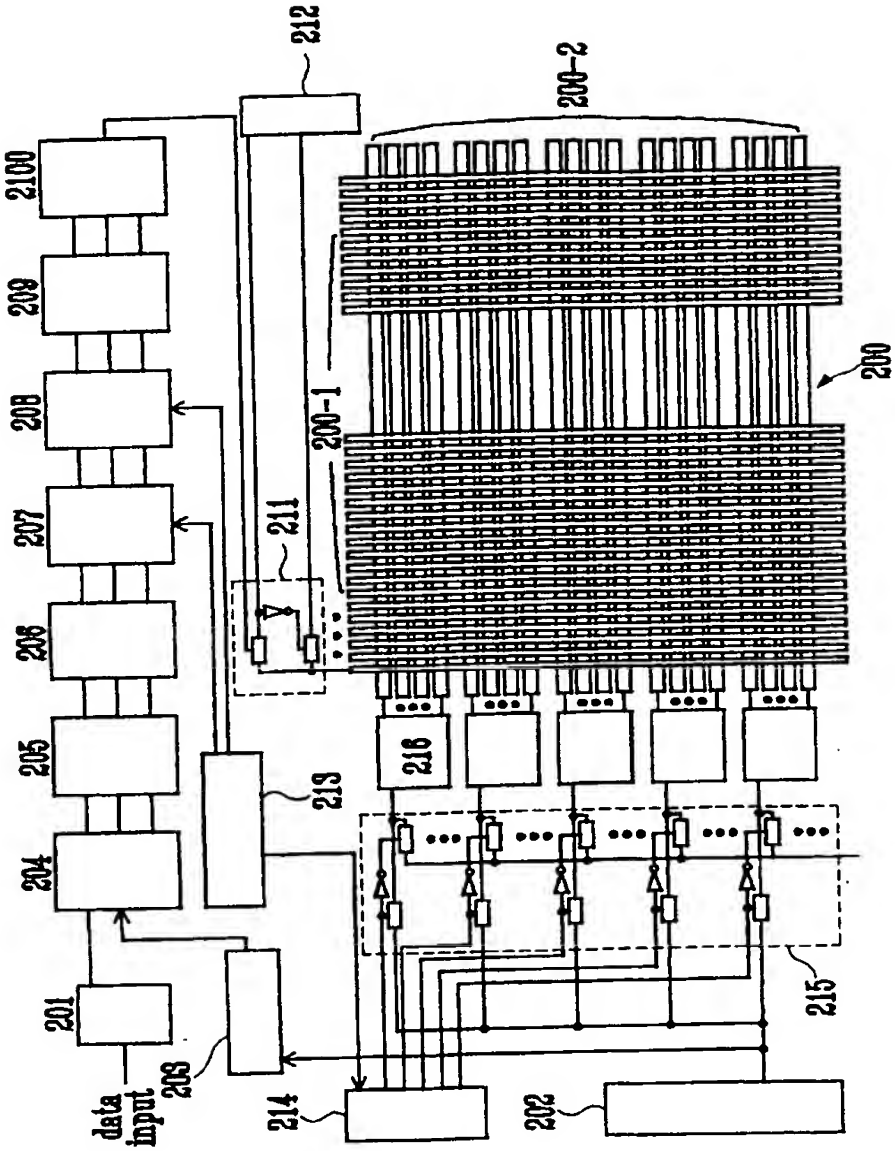
212
200-2
2100
209
208
207
206
205
204
201
data input
203
211
200-1
200
216
213
215
214
202

Fig. 7

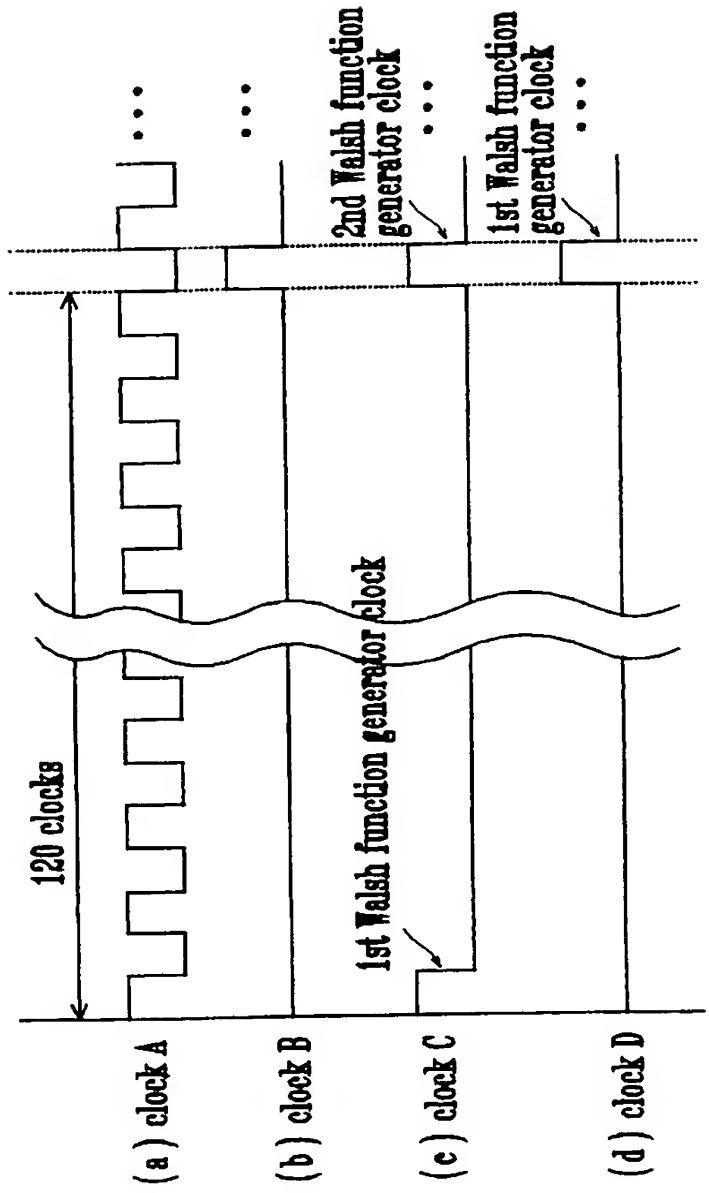
2nd Walsh function generator clock
1st Walsh function generator clock
120 clocks
1st Walsh function generator clock
(a) clock A
(b) clock B
(c) clock C
(d) clock D

Fig. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR 96/00228

A. CLASSIFICATION OF SUBJECT MATTER

IPC[6]: G 09 G 3/36

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC[6]: G 09 G 3/36

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

DERWENT WPIL

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 661 683 A1 (SEIKO INSTRUMENTS INC.) 05 July 1995 (05.07.95), abstract.	1
A	GB 2 186 414 A (SEIKO EPSON CORPORATION) 12 August 1987 (12.08.87), abstract.	1

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 February 1997 (28.02.97)	12 March 1997 (12.03.97)
Name and mailing address of the ISA/AT AUSTRIAN PATENT OFFICE Kohlmarkt 8-10 A-1014 Vienna Facsimile No. 1/53424/535	Authorized officer Kunze Telephone No. 1/53424/452

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/KR 96/00228

In Recherchenbericht angeführtes Patentdokument Patent document cited in search report Document de brevet cité dans le rapport de recherche	Datum der Veröffentlichung Publication date Date de publication	Mitglied(er) der Patentfamilie Patent family member(s) Membre(s) de la famille de brevets	Datum der Veröffentlichung Publication date Date de publication
EP A1 661683	05-07-95	JP A2 7199863	04-08-95
GB A 2186414		GB A0 8702297	11-03-87
		GB A1 2186414	12-08-87
		GB B2 2186414	01-11-89
		HK A 292/91	26-04-91
		JP B2 2572578	16-01-97
		KR B1 9101848	28-03-91
		SG A 601/90	07-09-90
		US A 4743096	10-05-88
		JP A2 62283321	09-12-87